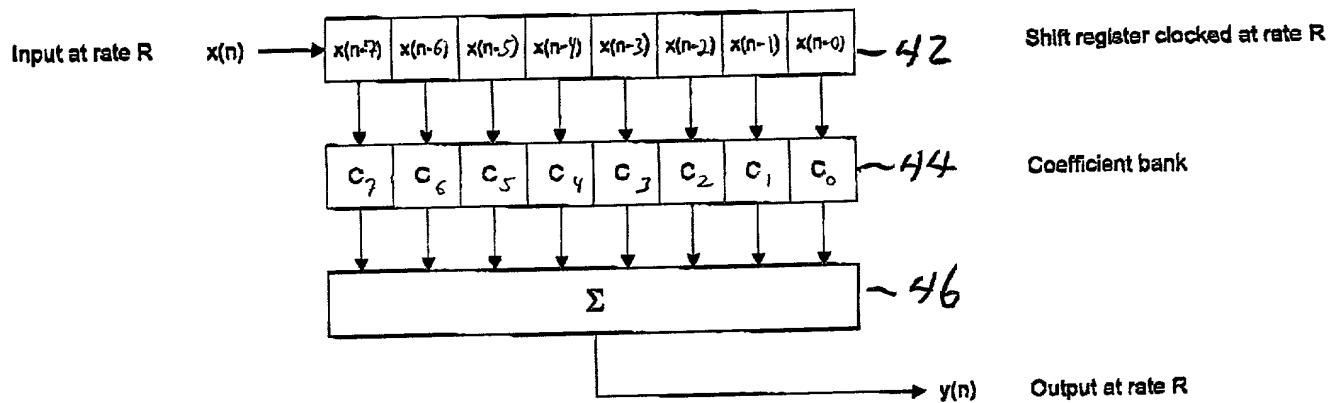


FIG. 1

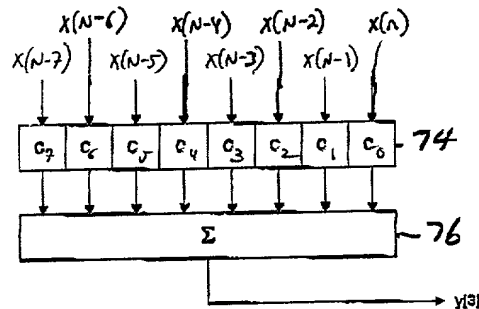
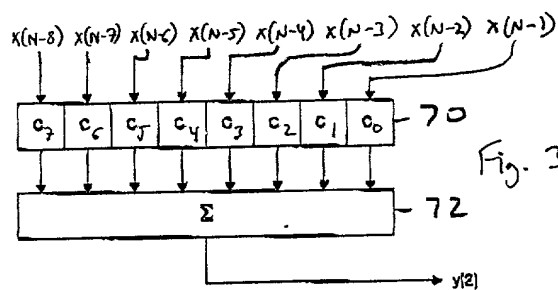
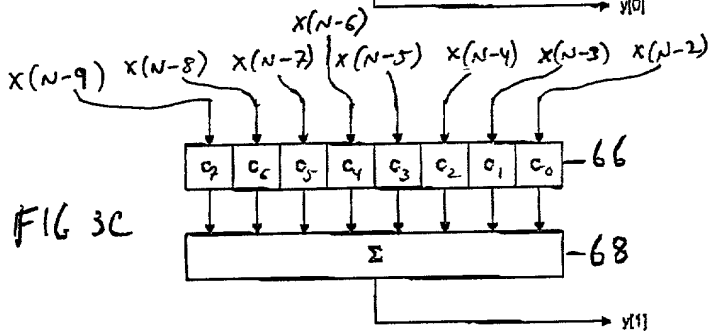
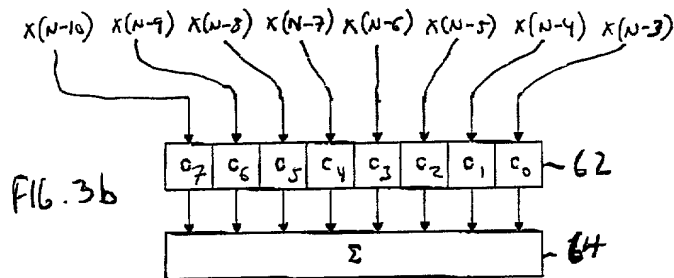
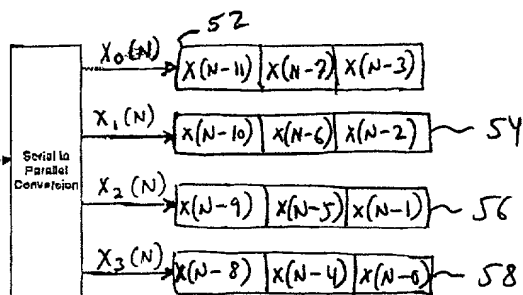


Serial Implementation of a FIR filter,
number of taps $K=8$.

Fig. 2

Input at rate R
Shift register clocked at rate R/4
Output at rate R/4

FIG 3a



**Parallel Implementation of a FIR filter,
number of taps $K=8$,
sample-to-clock rate ratio $N=4$.**